High κ dielectrics on InGaAs and GaN
- Growth, interfacial structural studies, and surface Fermi level unpinning

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Technical Milestones for 2010-2011:

1. ***growth of high dielectric constant oxides on InGaAs and GaN using molecular beam epitaxy (MBE) and atomic layer deposition (ALD)***
2. ***structural studies on hetero-structures of nano-thick Al_2O_3, HfO_2, and $Ga_2O_3(Gd_2O_3)$/ InGaAs (and GaN) using high-resolution x-ray reflectivity using in-situ/ex-situ high-resolution synchrotron radiation and high-resolution transmission electron microscopy***
3. ***correlation between electrical measurements and structural studies leading to the understanding of surface Fermi level pinning/unpinning***

We have successfully established and continuously kept our world-leading expertise of high κ dielectric growth using both molecular beam epitaxy (MBE) and atomic layer deposition (ALD) methods on InGaAs and GaN, including high κ enhancement, surface Fermi level unpinning in InGaAs, the equivalent oxide thickness (EOT) scaling to < 1 nm, the high temperature thermal stability, the fundamental study of the high-κ/InGaAs interfaces on their *electrical, chemical, and physical* properties, and the exploration of novel approach for high κ oxide growth. Furthermore, we have demonstrated world-record device performance and kept renewed the world-records in inversion-channel InGaAs MOSFETs and GaN MOSFETs without employing interfacial layers and surface chemical pre-treatments.

We have achieved many firsts and made great impacts in this important nano-electronics research, critical for novel digital electronic technologies beyond Si CMOS:

(1) Have achieved and continued to hold ***world record high*** dc performances of InGaAs MOSFETs, including the drain current, peak transconductance, and peak electron mobility in the self-aligned inversion-channel $In_{0.75}Ga_{0.25}As$ and $In_{0.2}Ga_{0.8}As$ MOSFETs using both *in-situ* MBE-Al_2O_3/GGO and *ex-situ* ALD-Al_2O_3 gate dielectrics. The high performance InGaAs MOSFETs will enable future digital transistor technology beyond Si CMOS.

(2) First to compare MBE-GGO and ALD-Al_2O_3 for InGaAs surface passivation by extracting the D_{it} distribution in the bandgap of InGaAs using conductance measurement at various temperatures. (ALD has been widely used in the Si industry for high κ gate dielectrics deposition and intensively studied for InGaAs surface passivation.)

(3) Discovery of effectively reduced D_{it} in GaAs MOSCAPs with a Ga-rich (4×6) reconstructed

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14. ABSTRACT
This is the report of a project to grow high dielectric constant oxides on InGaAS and GaN using molecular beam epitaxy and atomic layer deposition.

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CMOS, Gallium Nitride , Nanotechnology

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GaAs (001) surface compared to a As-covered c(4×4) reconstructed surface, vital for achieving a low D_{it} in GaAs MOSCAPs and realizing high performance GaAs MOSFETs.

(4) First to integrate *in-situ* ALD with MBE system and conduct thorough interfacial chemical analyses and electrical characterization of *in-situ* ALD Al_2O_3 on freshly MBE grown *n*- and *p*-GaAs (001) with (2×4) and (4×6) surface reconstruction.

(5) Have carried comprehensive studies of GGO and Gd_2O_3 on InGaAs using TEM, SPM, and synchrotron-radiation photoemission study.

(6) During 2007 to 2010, we have made strong impacts in the field, as evidenced from the number of citations of 1900 on our work.

(7) In 2010, we have given invited talks in China Semiconductor Technology International Conference (CSTIC), VLSI-TSA, European MRS, the 16th International Conference on Molecular Beam Epitaxy (MBE), the 4th AEARU Advanced Materials Science Workshop, SEMATECH Symposium, the 10th IEEE International Conference on Solid-State and Integrated Circuit Technology (ICSICT 2010), the Taiwan-Argonne Workshop on the Nano-Structured Materials, the 7th Taiwan/U.S. Air Force Nanoscience Workshop, and the NSRRC workshop, X-ray Investigation toward Nano-World. Our device work was also presented in 2010 Device Research Conference (DRC), European MRS, the 16th International Conference on Molecular Beam Epitaxy (MBE), APS March Meeting, and many conferences held in Taiwan.

1. Self-aligned inversion-channel InGaAs MOSFET

1.1. High-performance self-aligned inversion-channel $In_{0.75}Ga_{0.25}As$ MOSFETs using MBE-grown Al_2O_3/Ga_2O_3 (Gd_2O_3)

Chips integrating high κ's/InGaAs and /Ge onto Si substrates have become the leading candidates for complementary metal-oxide-semiconductors (CMOS) beyond the 15 nm node. Inversion-channel $In_{0.53}Ga_{0.47}As$ MOSFETs using molecular beam epitaxy (MBE)-Al_2O_3/ $Ga_2O_3(Gd_2O_3)$ [GGO] and atomic layer deposited (ALD)-Al_2O_3, with gate lengths (L_G) of 1 μm and 0.4 μm, respectively, have exhibited very high maximum drain currents ($I_{D\text{-}max}$) of 1.05 mA/μm.[1-3] In this work, using $In_{0.75}Ga_{0.25}As$ channel and MBE-Al_2O_3/GGO dielectrics, self-aligned inversion channel InGaAs MOSFETs have exhibited an even higher maximum drain current.

The 1μm-gate-length Al_2O_3/GGO/$In_{0.75}Ga_{0.25}As$ MOSFETs have achieved a maximum drain current of 1.23 mA/μm (Fig. 1), a peak transconductance of 464 μS/μm (Fig. 2) and a peak field-effect electron mobility of 1600 $cm^2/V{\cdot}s$ (Fig. 3). A new record of maximum drain current has been set, not only for III-V MOSFETs but also for all enhancement-mode MOSFETs with similar device dimensions, regardless of channel materials and device configurations. In addition, the devices have exhibit good gate length scalability (Fig. 4), which means the performance will be linearly improved by reducing the gate length. Fig. 5 summarizes the $I_{D\text{-}max}$ and $G_{m\text{-}max}$ of representative work on III-V enhancement-mode (E-mode) *n*-MOSFETs reported in the last decade, the maximum drain current of 1.23 mA/μm is the highest ever reported in all the E-mode III-V MOSFETs.

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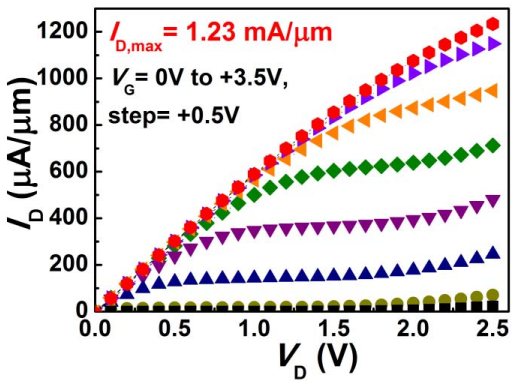

Fig. 1 I_D vs V_D of a 1μm-gate-length inversion-channel Al_2O_3/GGO/$In_{0.75}Ga_{0.25}As$ MOSFET, demonstrating an $I_{D\text{-}max}$ of 1.23 mA/μm at V_G = 3.5 V and V_D = 2.5 V.

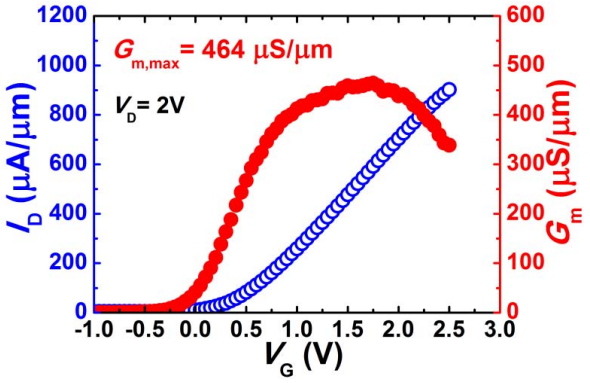

Fig. 2 Transfer characteristics and G_m curve of a 1μm-gate-length inversion-channel Al_2O_3/GGO/ $In_{0.75}Ga_{0.25}As$ MOSFET, exhibiting a $G_{m\text{-}max}$ of 464 μS/μm at V_G = 1.75V and V_D = 2V.

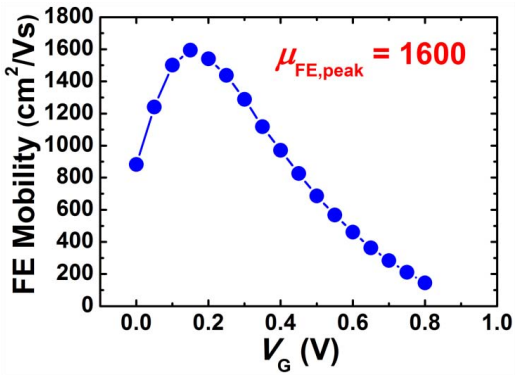

Fig. 3 Plot of field effective electron mobility of the inversion-channel Al_2O_3/GGO/$In_{0.75}Ga_{0.25}As$ MOSFETs.

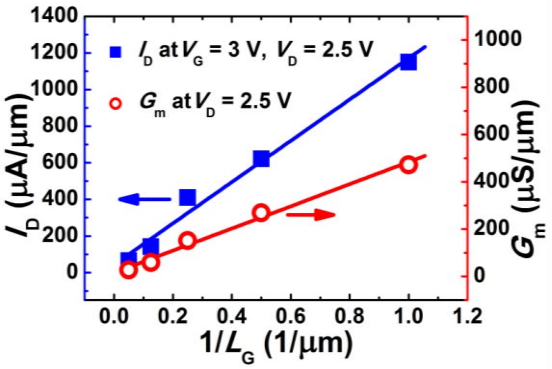

Fig. 4 $I_{D\text{-}max}$ at V_D = 2.5 V, V_G = 3 V and $G_{m\text{-}max}$ at V_D = 2.5 V versus inverse gate-length. Both properties are proportional to the inverse gate length.

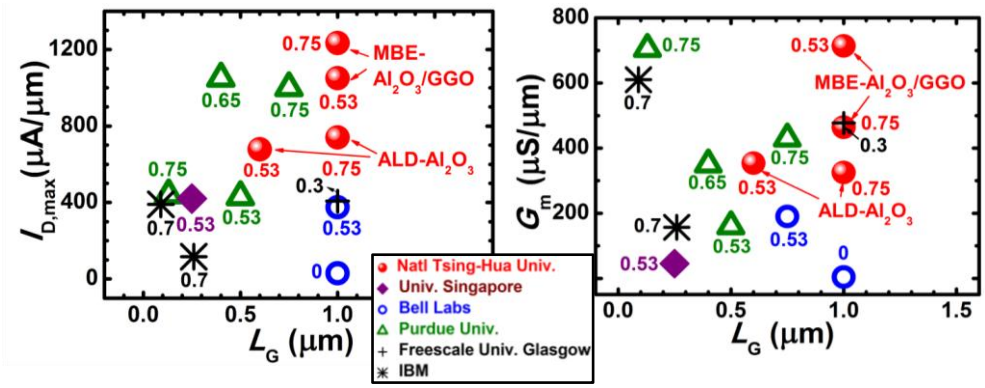

Fig. 5 Summary of (a) $I_{D\text{-}max}$ and (b) $G_{m\text{-}max}$ of representative work on III-V enhancement-mode *n*-MOSFETs reported in the last decade. The number near each data point indicates the In content (x) of the $In_xGa_{1-x}As$ channel used in corresponding device; x=0 stands for a GaAs channel. The self-aligned processed inversion-channel devices are denoted with solid circular and diamond symbols, and the data of non-self-aligned processed inversion-channel devices are denoted with hollow circular and triangular symbols. Symbols of cross and stars represent the data of non-inversion-channel (flat-band type or buried channel) E-mode MOSFETs.

1.2. High-performance self-aligned inversion-channel $In_{0.75}Ga_{0.25}As$ MOSFETs using ALD-Al_2O_3 - H. C. Chiu, P. Chang, M. L. Huang, T. D. Lin, Y. H. Chang, J. C. Huang, J. Kwo, and M. Hong

Figure 1(a) exhibits the I_D-V_D curves of a self-aligned inversion channel 1μm (L)× 50μm (W) $In_{0.75}Ga_{0.25}As$ MOSFET with 5nm-thick ALD-Al_2O_3 as gate dielectrics. A maximum I_D of 740 μA/μm was obtained under a gate bias of 2.5V and a drain bias of 2.5V. The device was fabricated with a self-aligned process similar to that used for the aforementioned Al_2O_3/GGO/$In_{0.75}Ga_{0.25}As$ MOSFET. The G_m curve measured from the same device is shown in Fig. 1(b). A maximum G_m of 325 μS/μm was demonstrated at V_D = 2V and V_G= 1.25V. A peak field-effect mobility of 490 $cm^2/V{\cdot}s$ was estimated from the transconductance analysis. Notice that the field-effect mobility is generally lower than the effective mobility extracted using split-CV method. A DIBL of 107 mV/V and a S.S. of 139 mV/decade were also obtained, as shown in Fig. 2. The threshold voltage extracted from a linear extrapolation is about 0.15V. In our previous work, 0.6-μm-gate-length ALD-Al_2O_3 (5-nm)/$In_{0.53}Ga_{0.47}As$ MOSFETs showed a maximum I_D of 678 μA/μm and a peak G_m of 354 μS/μm. In comparison, the $In_{0.75}Ga_{0.25}As$ MOSFET reported in this work exhibits maximum I_D and peak G_m of about 1.8 and 1.5 times, respectively, higher than those reported for the $In_{0.53}Ga_{0.47}As$ MOSFETs, while the Al_2O_3 thickness and the gate length are the same. The "extra" increments in I_D and G_m may be attributed to the $In_{0.75}Ga_{0.25}As$ channel. Fig. 3 summarizes the systematic dependence of maximum I_D and peak G_m on various gate lengths for ALD-Al_2O_3/ $In_{0.75}Ga_{0.25}As$ MOSFETs; the two values are proportional to the inverse gate length, $1/L_G$. Therefore, an improved performance is anticipated for devices with sub-micron gate-length; for example, a drain current of approaching 1.5 mA/μm for a 0.5μm-gate-length ALD-Al_2O_3/$In_{0.75}Ga_{0.25}As$ MOSFETs.

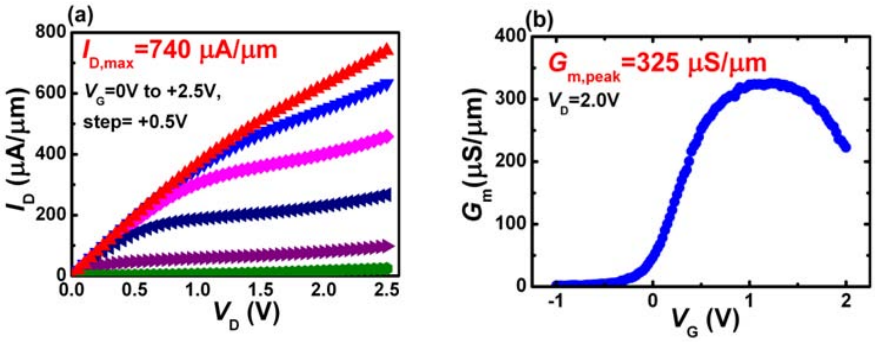

Fig. 1 (a) Output characteristics I_D vs V_D of an 1μm (L)×50μm (W) inversion-channel ALD-Al_2O_3/$In_{0.75}Ga_{0.25}As$ MOSFET. A maximum I_D of 740 μA/μm is measured at V_G=2.5V and V_D=2.5V; (b) The G_m curve of the same device showing a peak G_m of 325 μS/μm, measured at V_D =2V.

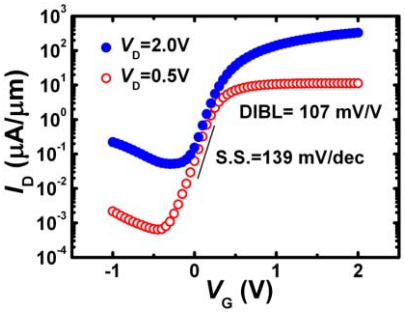

Fig. 2 Drain currents versus gate voltage of a 2μm (L)×100μm (W) inversion-channel ALD-Al_2O_3/ $In_{0.75}Ga_{0.25}As$ MOSFET measured at drain voltages of 0.5V and 2V, respectively, showing a DIBL of 107 mV/V and a S.S. of 139 mV/decade. =2V.

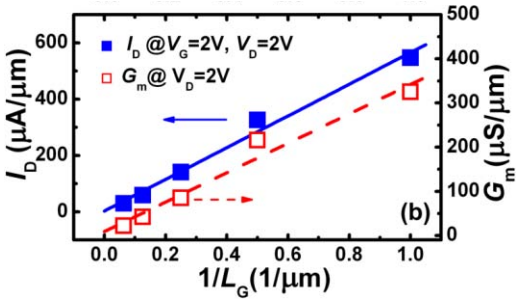

Fig. 3 Drain current and peak transconductance versus inverse gate-length ($1/L_G$) for ALD-Al_2O_3/ $In_{0.75}Ga_{0.25}As$ MOSFETs. Both properties are proportional to the inverse gate length.

1.3. Self-aligned inversion-channel $In_{0.20}Ga_{0.80}As$ MOSFETs using *in-situ* MBE-Al_2O_3/GGO

A 4μm-gate-length MOSFET using a gate dielectric of Al_2O_3 (3 nm thick)/GGO (8 nm thick) demonstrates a maximum drain current of 9.5 μA/μm, and an extrinsic transconductance of 3.9 μS/μm (Fig.1). The linear dependence of the maximum drain current and the peak transconductance with the inverse gate length is observed for devices with various gate lengths, as shown in Fig. 2. Maximum drain current and peak transconductance presented above are compared favorably with representative published work for GaAs-based surface channel NMOSFETs with low indium content are summarized in Fig. 3.[2,4,5]

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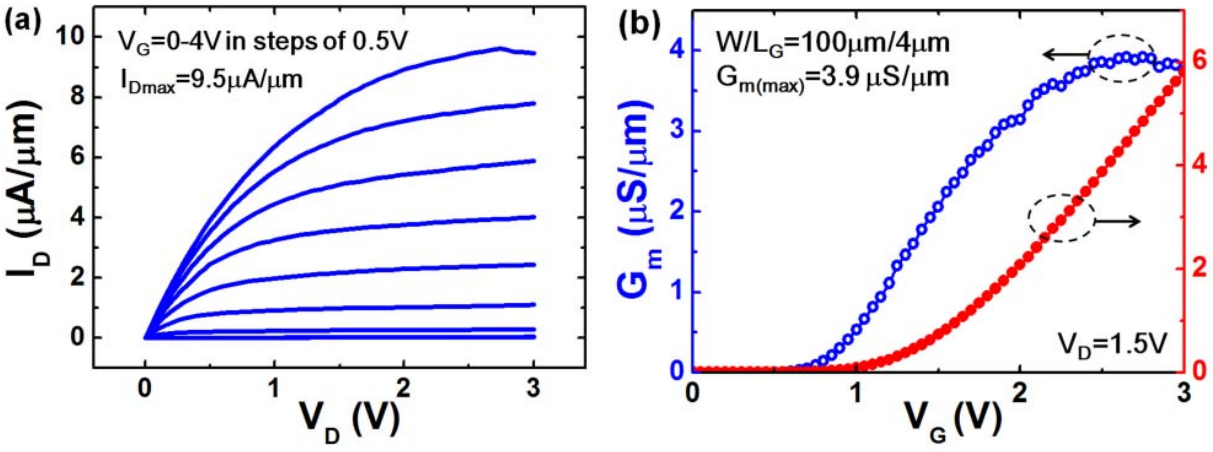

Fig. 1 (a) I_D-V_D characteristics (b) I_D-V_G characteristics and transconductance G_m curve of an inversion channel $In_{0.2}Ga_{0.8}As$ MOSFET (W/L = 50 μm/4μm).

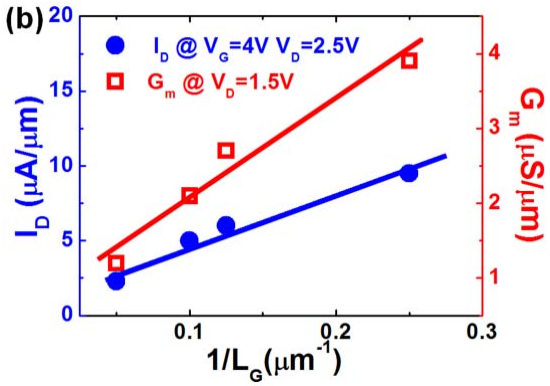

Fig. 2 Maximum drain current and peak transconductance versus gate lengths demonstrate a linear dependence.

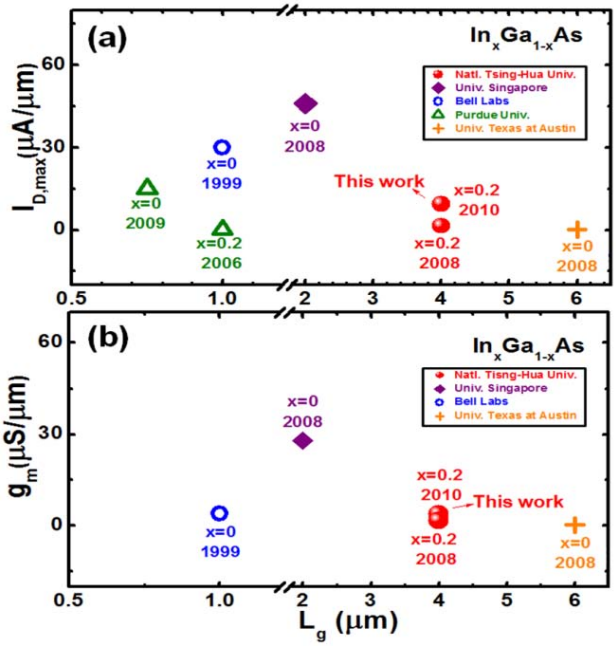

Fig. 3 The comparison of (a) maximum drain current and (b) peak transconductance of representative work on GaAs-based low indium content surface channel NMOSFET reported previously.

3. D_{it} distributions within InGaAs bandgaps

3.1. Low interfacial density of states around mid-gap in MBE-GGO/ $In_{0.2}Ga_{0.8}As$ (in collaboration with IMEC)

In this work, the D_{it} distribution within the band-gap of $In_{0.2}Ga_{0.8}As$ was plotted only from the measured results with the gate bias in the depletion region. With the conductance measurements at room temperature, D_{it} shows values of ~$5x10^{11}eV^{-1}cm^{-2}$ above and $2x10^{12}eV^{-1}cm^{-2}$ below the midgap region for the MBE-GGO/InGaAs; In the mid-gap region (the energy 0.5-0.7 eV above the valence band edge), the D_{it} values with a mean of less than $5x10^{12}eV^{-1}cm^{-2}$ were obtained at 100 and 150°C, which may mainly be due to the temperature-induced traps.(Fig. 1)

As to the ALD-Al_2O_3 case, the D_{it} values around the midgap region are larger than those of the MBE-GGO samples. The higher D_{it} values can be elucidated from the low-frequency C-V curves at 150°C, in which a "dip" capacitance in the depletion region is higher for ALD-Al_2O_3 case than that for MBE-GGO sample. In general, a lower "dip" capacitance in the depletion region for low frequency C-V curves reveals a smaller D_{it} value. A similar D_{it} distribution with noticeable peak-like features near the midgap region was also observed in the ALD-Al_2O_3/ GaAs. (Fig. 2)

The D_{it} distribution may explain the device performances in inversion-channel InGaAs MOSFETs because the Fermi level is driven across the mid-gap to invert the minority carriers. In these two cases[1,2], the different device performances of the two inversion-channel InGaAs

MOSFETs have the strong correlations with the D_{it} distribution around the mid-gap. Beside the *ex-situ* ALD Al_2O_3 as mentioned earlier, more recently, we have also finished the electrical characterization for the *in-situ* ALD Al_2O_3 on III-V substrates, including $In_{0.2}Ga_{0.8}As$ and GaAs with different (4x6) and (2x4) surface reconstructions for both *n*- and *p*- types, respectively. (Fig. 3) The results are under analysis and discussion.

References

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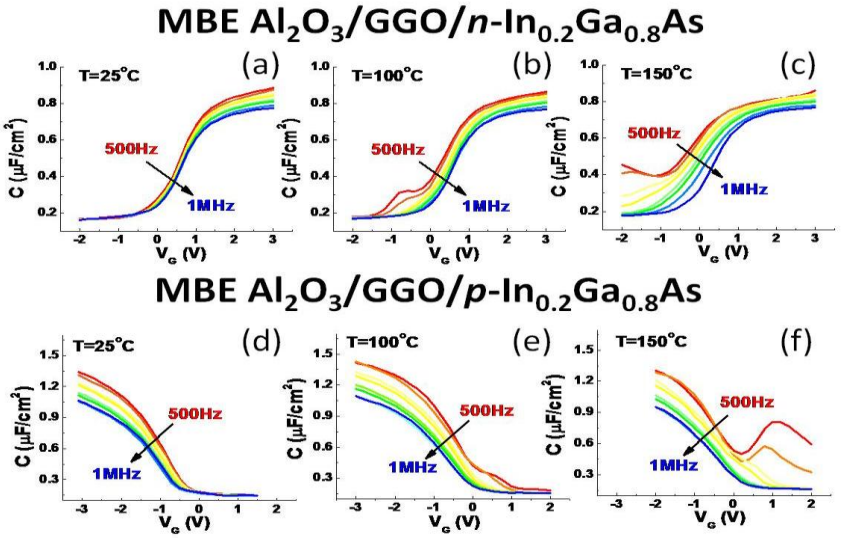

Fig. 1 Capacitance-voltage (C-V) curves of MBE-Al_2O_3/GGO/$In_{0.2}Ga_{0.8}As$ gate stack with varying temperature: (a) 25°C (b) 100°C (c) 150°C of *n*-$In_{0.2}Ga_{0.8}As$; and (d) 25°C (e) 100°C (f) 150°C of *p*-$In_{0.2}Ga_{0.8}As$.

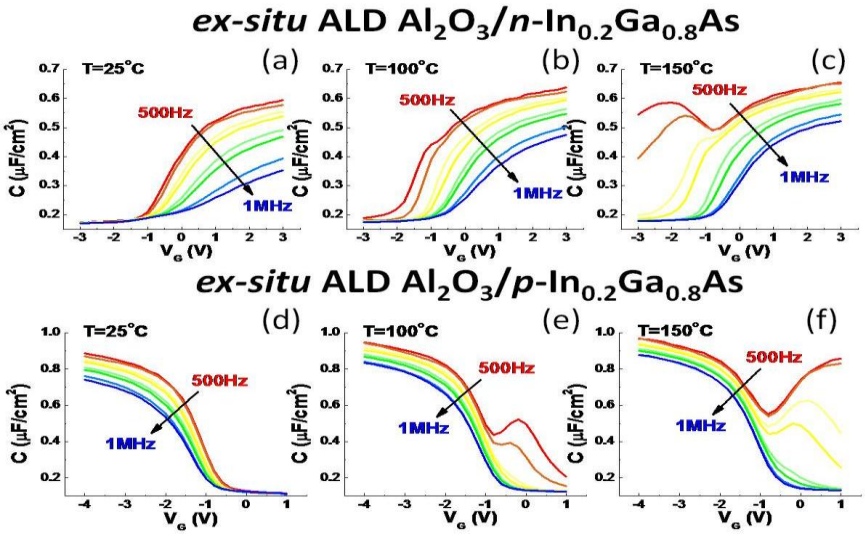

Fig. 2 Capacitance-voltage (C-V) curves of ALD-Al_2O_3/$In_{0.2}Ga_{0.8}As$ gate stack with varying temperature: (a) 25°C (b) 100°C (c) 150°C of *n*-$In_{0.2}Ga_{0.8}As$; and (d) 25°C (e) 100°C (f) 150°C of *p*-$In_{0.2}Ga_{0.8}As$.

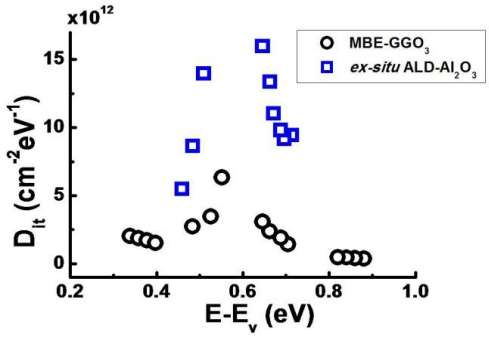

Fig. 3 Comparisons of D_{it} vs trap energy level of MBE-Al_2O_3/GGO/$In_{0.2}Ga_{0.8}As$ and ALD-Al_2O_3/$In_{0.2}Ga_{0.8}As$, derived using temperature-dependent conductance method.

3.2. Effective reduction of interfacial traps in Al_2O_3/GaAs (001) gate stacks using surface engineering and thermal annealing - (in collaboration with IMEC)

C-V characteristics of Al_2O_3/*p*-type GaAs MOSCAPs (with a Ga-rich surface reconstruction) annealed under various conditions have been summarized in Fig. 1: (a) annealing at 550°C for 20 minutes, (b) at 550°C for 60 minutes, (c) 550°C for 60 minutes followed by 650°C for 30 seconds, (d) 550°C for 60 minutes followed by 650°C for 20 minutes, and (e) 550°C for 60 minutes followed by 750°C for 30 seconds. All the C-V curves denoted as (I) were measured at 25°C, and are well behaved with almost identical characteristics for various annealing conditions. This is because only a small range of interfacial traps with energies of 0.3-0.5 eV lying above the valence band edge (E_v) in these samples was probed at 25°C and the measured D_{it}'s are nearly the same of ~low 10^{12} $eV^{-1}cm^{-2}$ in this narrow region. In contrast, C-V measurements denoted as (II) were performed at 150°C, probing the interfacial traps covering the mid-gap region. Pronounced trap-induced capacitance responses, manifested as the "hump" located in the depletion region, were observed at the low frequencies, consistent with those reported previously.

As shown in Fig. 1(II), annealing condition (b) and (c) show much smaller humps than those of (a), (d) and (e), indicating an improved interfacial quality. These results reveal that the long-time annealing at a medium temperature of 550°C helps to reduce the hump (Fig. 1(a), (b)), and the annealing at 550°C for 60 minutes followed by 650°C for 30 seconds (Fig. 1(c)) is the optimized annealing condition responsible for the lowest values of D_{it} (Fig. 3(a)) and the smallest frequency dispersion in depletion. The heat treatments of a prolonged duration at 650°C and/or at higher annealing temperature, such as 650°C for 20 minutes (Fig. 1(d)) or 750°C (Fig. 1(e)), tend to deteriorate the interfacial quality. Recent XPS study on the Al_2O_3/GaAs interface revealed the inter-diffusion of Ga into Al_2O_3 at elevated temperatures over 750°C. Nevertheless, all the Al_2O_3/GaAs MOSCAPs demonstrated low gate leakage current densities at V_{fb}-1V under various annealing conditions (not shown), which are lower than 10^{-7} A/cm^2 and 10^{-6} A/cm^2, measured at 25°C and 150°C, respectively, suggesting the good insulating property of Al_2O_3 is still maintained.

Fig. 2 shows the C-V characteristics of MOSCAPs of Ga-rich and As-covered samples of both *p*- and *n*-type, treated with the optimized annealing condition described above. As expected, all the corresponding C-V results at 25°C show negligible differences. The C-V at 150°C of the samples with a c(4x4) reconstructed, As-covered surface show larger humps measured for both *p*-type (Fig. 2(c)) and *n*-type substrates (Fig. 2(d)), giving substantially higher D_{it} near the mid-gap by nearly

one order of magnitude than the samples on the Ga-rich surface.

Systematic post anneals of MOSCAPs grown on the As-covered GaAs surface of c(4x4) reconstruction led to only slightly reduction of D_{it} shown in Fig. 3(a). The post annealing process optimized for the Ga-rich surface appears to be rather ineffective to improve the interfacial quality of the samples with As-covered. The D_{it} near the mid-gap still exceeds 10^{13} $eV^{-1}cm^{-2}$ for the As-covered sample. In contrast, a significant reduction of D_{it} to ~$2x10^{12}$ $eV^{-1}cm^{-2}$ near the mid-gap region ($E\text{-}E_v$=0.7 eV) is clearly demonstrated on Ga-rich samples after the optimized anneal. The D_{it} spectra of Al_2O_3/GaAs gate stacks grown on the Ga-rich and the As-covered surfaces are plotted in Fig. 3(b), showing a peak value of low 10^{12}, and 10^{13} $eV^{-1}cm^{-2}$, respectively, in sharp contrast to a "U" shaped D_{it} for SiO_2/Si with a mean value in low 10^{10} $eV^{-1}cm^{-2}$.

In summary, a significant reduction of the mid-gap peak in D_{it} has been demonstrated for the first time in Al_2O_3/GaAs MOSCAPs by employing *in-situ* MBE oxide growth on a Ga-rich (4x6) reconstructed GaAs (001) surface as opposed to the As-covered c(4x4) reconstructed surface, followed by an optimized thermal annealing at 550°C for 60 minutes and 650°C for 30 seconds.

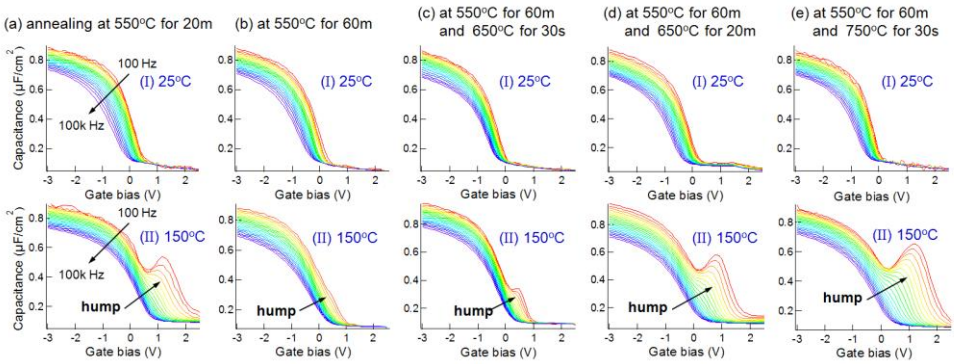

Fig. 1 Capacitance-voltage (C-V) measurements on Ni/Al_2O_3(9nm)/*p*-type GaAs MOS capacitors (MOSCAPs) with Ga-rich GaAs reconstructed surface: (I) C-V curves measured at 25°C, and (II) C-V curves measured at 150°C.

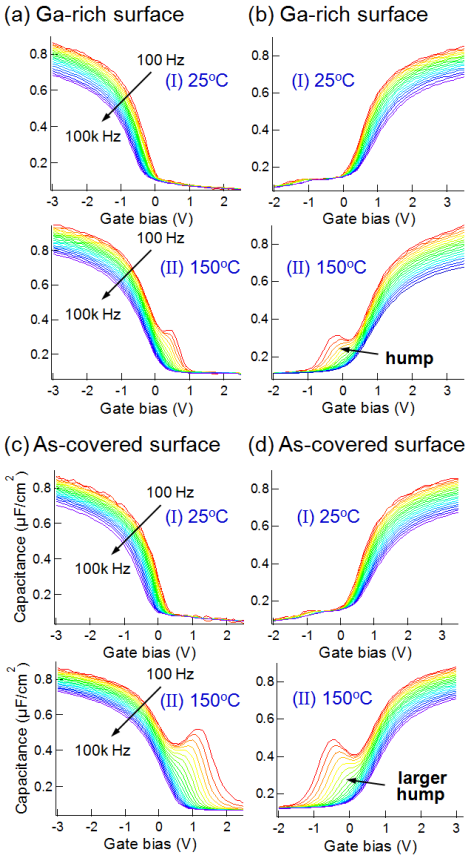

Fig. 2 C-V curves of GaAs MOSCAPs started with Ga-rich surface on (a) *p*-type and (b) *n*-type substrates, and started with As-covered surface on (c) *p*-type and (d) *n*-type substrates.

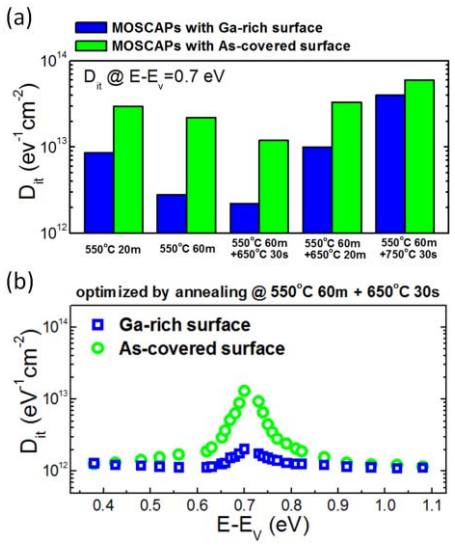

Fig. 3 (a) Comparison of D_{it} on various annealing temperatures and dwelling durations, and (b) D_{it} distribution as a function of the energy above E_v for GaAs MOSCAPs prepared on the Ga-rich and As-covered surfaces.

4. In-situ ALD

Electrical properties and interfacial chemical environments of *in-situ* atomic layer deposited Al_2O_3 on freshly molecular beam epitaxy grown GaAs

C-V curves of ALD-Al_2O_3/p-GaAs with small dispersions at accumulation have been reported by several groups using various surface treatments.[1-4] However, all C-V characteristics of ALD-Al_2O_3/n-GaAs exhibit much more pronounced frequency dispersion.[1-4]

In this work, hetero-structures of ALD-Al_2O_3 on freshly MBE-GaAs were grown in a multi-chamber MBE/ALD/XPS system. These chambers are connected with transfer modules in 10^{-10} Torr. Note that no surface treatments and interfacial passivation layers were employed.

Figure 1 (a) and (b) show the *in-situ* Ga $2p_{3/2}$ and As $2p_{3/2}$ core level spectra of 1nm ALD-Al_2O_3/n-GaAs. As can be seen in Fig. 1 (a), the asymmetric line shape of the Ga $2p_{3/2}$ core suggests the existence of a feature embedded in the measured spectrum. A fit reveals then its position lying about 0.63 eV below the bulk GaAs, which corresponds to the Ga^{1+} state (Ga_2O). As to the As $2p_{3/2}$ core, Fig. 1(b) exhibits the fitted result which shows a structure located in a higher EB of about 0.70 eV than that of the bulk GaAs. It corresponds to emission from the As-As bonding (As^0). Notice that neither arsenic oxides (the As^{3+} (As_2O_3) and As^{5+} (As_2O_5) states) nor gallium oxide (the Ga^{3+} (Ga_2O_3) state) were detected.

Similar measurements on a ALD-Al_2O_3/p-GaAs sample are plotted in Fig. 1(c) (Ga $2p_{3/2}$) and (d) (As $2p_{3/2}$) in green open circles. No major difference in interfacial chemical environments between ALD-Al_2O_3/n- and p-GaAs can be distinguished, as shown in Fig.1 (c) and (d). The results indicate that the disparity between ALD-Al_2O_3/n- and p-GaAs may not be due to different interfacial chemical bonding; further, they suggest that As^0 and/or Ga^{1+} may be the reason for the disparity in C-V characteristics.

An *in-situ* ALD-Al_2O_3(8 nm)/n-GaAs hetero-structure, the same sample for the C-V measurements, was adopted to study the chemical bonding environments of ALD-Al_2O_3/GaAs interface before and after 550°C annealing in N_2 for 1hr. The XPS spectra of the As *3d* and Ga *3d* of the as-deposited and the annealed samples are shown in Fig. 2 (a)-(c). The As-related bonding at interface remained unchanged after the 550°C N_2 annealing, by comparing As *3d* spectra between the as-deposited and the annealed samples, as shown in Fig. 2 (a). No arsenic oxide (As_2O_3 or As_2O_5) was detected after the annealing. Fig. 2 (b) and (c) show the comparison and the de-convoluted results of O 2s and Ga *3d* spectra between the as-deposited and the annealed samples. No additional bonding other than Ga-As and Ga^{1+} in the annealed sample can be found, further confirming that the interfacial bonding remained unchanged after the annealing.

Fig. 3 (a)-(d) show the C-V characteristics (100 Hz-100k Hz) of the as-deposited and 550°C N_2 annealed n- and p-GaAs MOSCAPs. C-V curves with frequency dispersions (< 5%) at accumulation were obtained in both p-GaAs MOSCAPs. The as-deposited n-GaAs MOSCAP gave a much pronounced frequency dispersion, which was reduced after 550°C N_2 annealing.

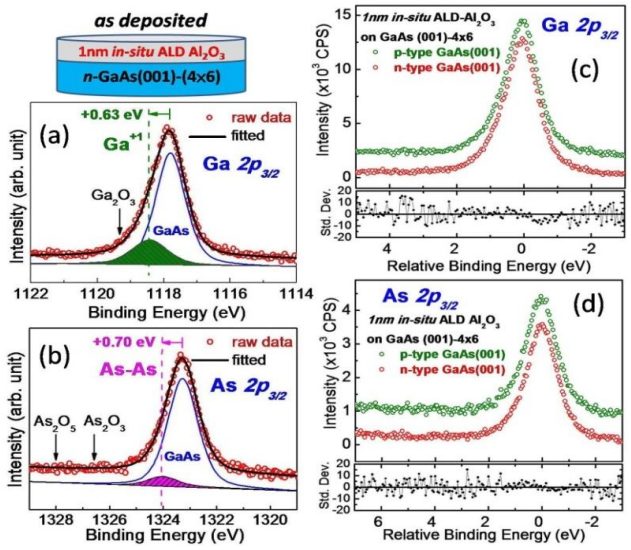

Fig.1 *in-situ* XPS (a) Ga $2p_{3/2}$ and (b) As $2p_{3/2}$ spectra of 1nm *in-situ* ALD-Al_2O_3/n-GaAs (001). (c) Ga $2p_{3/2}$ and (d) As $2p_{3/2}$ raw spectra along with corresponding difference-curves were illustrated for the direct comparison.

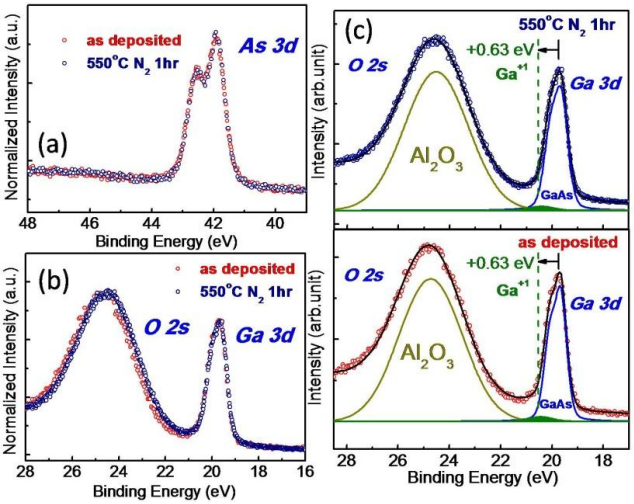

Fig. 2 Comparison of XPS (a) As *3d* and (b) Ga *3d* and O *2s* spectra of 8 nm *in-situ* ALD-Al_2O_3/n-GaAs before and after 550°C N_2 annealing for 1hr. (C) De-convoluted results of Ga *3d* and O *2s* spectra of as-deposited and 550°C N_2 annealed samples.

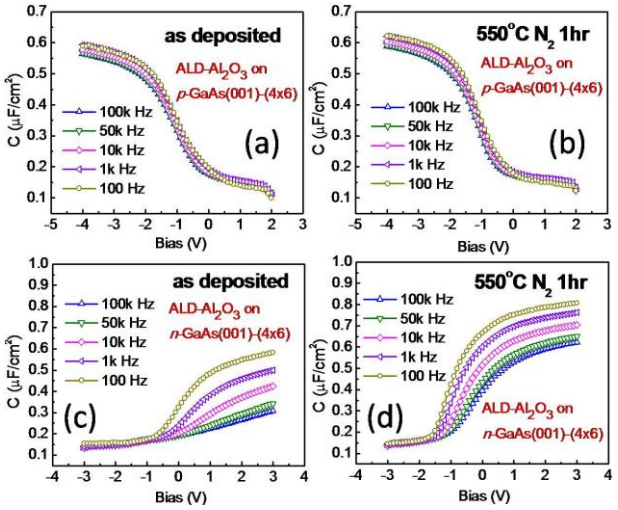

Fig. 3 C-V characteristics of (a) as deposited (b) 550°C N_2 annealed *in-situ* ALD-Al_2O_3/ p-GaAs and (c) as deposited (d) 550°C N_2 annealed *in-situ* ALD-Al_2O_3 /n-GaAs.

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5. Interfacial studies on high k's/InGaAs - TEM

GGO on $In_{0.2}Ga_{0.8}As$

Complementary to the averaged structural information over a large probed area provided by x-ray scattering measurements, typical of a few mm^2, TEM micrographs yield detailed information about the local structure. Figure 1 shows the HRTEM micrograph of Al_2O_3/GGO/$In_{0.2}Ga_{0.8}As$/GaAs heterostructure with different GGO film thickness from 11 nm, 6 nm, 4.5 nm, and 3 nm ((a), (b), (c), and (d), respectively) before RTA treatment viewed along [110] zone axis, where the interface between GGO and $In_{0.2}Ga_{0.8}As$ is atomically sharp and smooth.

A HRTEM image of Al_2O_3/GGO/$In_{0.2}Ga_{0.8}As$/GaAs heterostructure with GGO 4.5 nm film thickness after RTA treatment viewed along [110] zone axis, where the interface between GGO and $In_{0.2}Ga_{0.8}As$ remains atomically sharp and smooth (shown in Fig. 2). Some crystalline lattice fringes were observed in GGO films. A 1-D fast Fourier transform (FFT) image of the framed covers the $In_{0.20}Ga_{0.80}As$/GaAs interface is shown in the inset of Fig. 2. Only the in-plane (-220) and (2-20) diffraction spots were used to obtain the image. The (2-20) crystal plane exhibits continuity across the InGaAs/GaAs interface and no misfit dislocations were observed at the interface. It indicates that strain relaxation did not take place after the high temperature RTA. The examination has been applied to many areas in the TEM specimen. All the results indicate that the InGaAs remains strained and dislocation-free after the 850°C RTA.

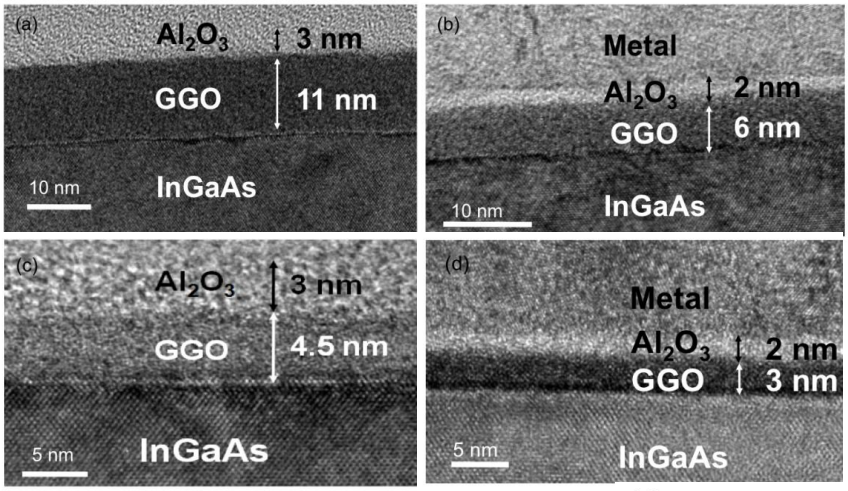

Fig. 1 HR-TEM images of Al_2O_3/GGO/$In_{0.2}Ga_{0.8}As$/GaAs heterostructures with different GGO film thickness (a) 11 nm (b) 6 nm (c) 4.5 nm (d) 3 nm.

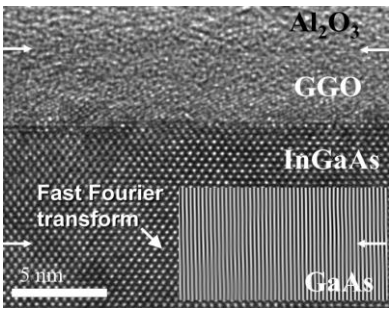

Fig. 2 HR-TEM image of Al_2O_3/GGO/ $In_{0.2}Ga_{0.8}As$/GaAs was taken after thermal treatment. The interface is marked with the arrows. Fast Fourier transform image of the framed area, by using the in-plane (-220) and (2-20) reflections, is shown as an inset.

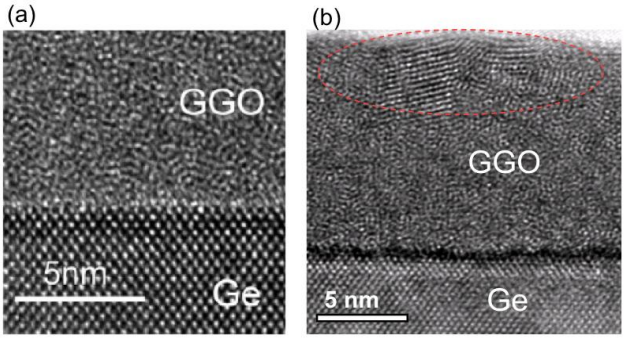

Fig. 3 HRTEM images of (a) before and (b) after a CF_4 plasma treatment and a 500°C-N_2-annealing.

6. Conclusion

The continuous scaling of transistors, which in the past has provided high-density, low-cost, and high-performance Si integrated circuits (ICs), does not guarantee device performance advantages. New materials and innovative device architectures become the key for reaching the required performance and continuing CMOS scaling. The replacement of the long-standing, reliable combination of SiO_2 and ploy-silicon gates with HfO_2-based high κ dielectrics and metal gates in the 45, 32, and 22 nm node technologies has opened the possibility of using alternative materials to

supplant the active strained-Si channel. Looking ahead beyond the 15 nm node ICs, the general consensus is to integrate MOSFETs using high-κ/metal-gates and high mobility channels, such as InGaAs and Ge, with the Si substrates to for realizing high performance and low power CMOS.

Fundamental research and developments are urgently demanded for realizing the revolutionary CMOS technology by year 2015-2017. Our NTHU research team have successfully established and continuously kept our world-leading expertise of high κ dielectric growth using both MBE and ALD approaches on the high mobility channel materials of InGaAs and Ge. We have achieved many firsts and made great impacts in this important nano-electronics research, critical for extending the digital technology beyond Si CMOS.

Our latest achievements and advances in high κ's on high mobility channels in the year 2010 include continuing to push the world-records in inversion-channel InGaAs MOSFETs and Ge MOSFETs without employing interfacial layers and surface chemical pre-treatments, EOT scaling of high κ's on InGaAs and Ge to < 1 nm, fundamental study of the high-κ/InGaAs and high-κ/Ge interfaces on their electrical, chemical, and physical properties, integration of *in-situ* ALD with MBE system, comprehensive study and comparison of MBE and ALD oxides on InGaAs and Ge.

Based on what we have accomplished during the past three years (2008-2010), supported by AOARD and many other funding agencies in Taiwan and internationally, we are confident that our NTHU team, with the close collaboration with domestic and international research institutions, will achieve even more in nano-electronics in the coming years.